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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,583	02/05/2004	Douglas A. Larson	501296.01 (30266/US)	6732

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EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,583	LARSON ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-43 are in the application.

Claims 1-43 are rejected.

Claim Objections

Claims 10,20,31,37 are objected to because of the following informalities:

The recitation of "the first set of data" and "the second set of data.." lack antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,5,11,16,21,26,32,34,36,38,40 rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US 2005/0105350) and in view of Zumkehr (US 6901494).

As in claim 1, Zimmerman describes a memory hub for a hub-based memory module (Zimmerman's Fig 2: MMB, paragraph 17), comprising: first and second link interfaces for coupling to respective data busses; a data path coupled to the first and second link interfaces and through which data is transferred between the first and second link interfaces (Zimmerman's Fig 2, links 112 on both sides of MMB; paragraphs 15); the claim further recites and a write bypass circuit coupled to the data path to couple write data on the data path and temporarily store the write data to allow read data to be transferred through the data path while the write data is temporarily stored. Zimmerman does not describe the claim's detail of the write bypass circuit. However, Zumkehr describes a memory controller hub circuits (Fig 3: #220) with a write buffer that can defers a write data transfer (Fig 5, T5B, write command 520A deferring writing to sdram devices), temporary stored in the write buffer (Fig 5, T5B), while allowing the read data command from sdram devices transferred from sdram devices to the memory controller (Fig 6, T3B to T5B). It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory controller hub circuits and methods as suggested by Zumkehr in Zimmerman's system to allow transferring read data while temporary storing write data, thereby resulting in more efficiently usage of the memory bus in the system (Zumkehr's column 6 lines 35-60).

Claim 11 rejected based on the same rationale as in the rejection of claim 1.

Claims 2-10,12-43 rejected under 35 U.S.C. 103(a) as being unpatentable over Zimmerman (US 2005/0105350), Zumkehr (US 6901494) as applied to 1 and in view of Garcia et al (US 6782435).

As in claim 2, the claim recites wherein the write bypass circuit comprises: a multiplexer having a first input coupled to the data path and further having a second input, an output, and a selection terminal, the multiplexer coupling the output to the first or second input in accordance with a selection signal applied to the selection terminal; a first-in-first-out (FIFO) register having an input coupled to the data path and further having an output coupled to the second input of the multiplexer; an output buffer having a buffer input coupled to the output of the multiplexer and further having a buffer output and an activation terminal, the output buffer coupling the buffer input to the buffer output in accordance with an activation signal applied to the activation terminal; and a selection circuit coupled to the multiplexer to generate the selection signal and activation signal when activated to couple the second input of the multiplexer to the output of the multiplexer. The claim rejected based on the same rationale as in the rejection of claim 1. Zimmerman and Zumkehr do not explicitly describe the claim's multiplexer. However, Garcia's Fig 2 describes a multiplexer, a bypass selection signal, and a register to temporary store write data being received. It would have been obvious to one of ordinary skill in the art at the time of invention to include the temporary storage and the multiplexer circuits as suggested by Garcia in Zimmerman's system to temporary reordering the transmitting data thereby allowing accessing memory device with minimum latency and maximizing the throughput of he overall system (Garcia's column 1, lines 48-62).

As in claims 3, the claim recite wherein the write bypass circuit further comprises an input buffer having an input coupled to the data path and an output coupled to the inputs of the multiplexer and the FIFO register. The claim rejected based on the same rationale as in the rejection of claim 2.

As in claim 4, Zimmerman's Fig 5 describes a memory device interface coupled to the data path, the memory device interface for coupling data to at least one memory device to which the memory device interface can be coupled.

Claims 5,16 recites the limitations of claims 1 and 2, therefore the claim is rejected based on the same rationale as in claims 1 and 2. The switching circuits and the data bypass circuits correspond to the multiplexer circuits and data bypassing circuits described in claim 2.

Claims 6,12,17,22,27 rejected based on the same rationale as in the rejection of claim 2.

Claims 7,13,18,23,28 rejected based on the same rationale as in the rejection of claim 3.

Claims 8,14,19,24,29 rejected based on the same rationale as in the rejection of claim 4.

As in claim 9, the claim recites wherein the memory device interface comprises: a memory controller coupled to the data path through a memory controller bus and further having a memory device terminal to which a memory device can be coupled; a write buffer coupled to the memory controller for storing memory requests; and a cache coupled to the memory controller for storing data. The claim rejected based on the same rationale as in the rejection of claim 1. Zimmerman further describes the CPU in Fig 1: #101 represents a general microprocessors for executing Intel's instruction sets. Furthermore the microprocessor has been known in the art having caches to store instructions and data for its execution in an efficiently manner.

As in claim 10, the claim recites wherein the first set of data represents write data and the second set of data represents read data. The claim rejected based on the same rationale as in the rejection of claims 1 and 2.

As in claim 15, the claim recites wherein the memory device interface of the memory hub comprises: a memory controller coupled to the data path through a memory controller bus and further coupled to at least one of the plurality of memory devices through a memory device bus; a write buffer coupled to the memory controller for storing memory requests directed to the memory device coupled to the memory controller; and a cache coupled to the memory controller for storing data provided to the memory device or retrieved from the memory device. The claim rejected based on the same rationale as in the rejection of claims 9 and 4. Zumkehr shows the memory device bus as in Fig 3: #161.

Claims 25,30 rejected based on the same rationale as in the rejection of claim 9.

Claims 20,31,33,37 rejected based on the same rationale as in the rejection of claim 10.

Claim 21 rejected based on the same rationale as in the rejection of claim 5. Zumkehr 's Fig 1 further shows a system comprising processor (Fig 1: #101), system controller (Fig 1: #111, #121), i/o devices (Fig 1: # 135-139).

Claim 26 rejected based on the same rationale as in the rejection of claim 21.

Claim 32 recites the write bypass method that is described in claim 1. Therefore, claim 32 is rejected based on the same rationale as in the rejection of claim 1.

As in claim 34, Zumkehr describes translator circuit to translate a write command to an sdram write command for the memory device, in addition to the FIFO queue for other write commands being received (Zumkehr's column 5 lines 5-12).

As in claim 35, the claim recites wherein the memory system includes a plurality of memory modules coupled in series on the memory bus, and writing the write data to the memory location comprises writing the write data to a memory location located in a memory module located downstream of the memory module from which the read data was accessed. Zimmerman's paragraphs 16-17 describe the point-to-point topology that the MMB of the upstream passing data to the downstream MMB.

Claim 36 describes the sequence of steps for the write bypassing method. The claim recites the situation when the write command is deferred to allow the read to go thru (see Zumkehr's Fig 5, T5B). It's rejected based on the same rationale as in the rejection of claim 5.

As in claim 38, Zumkehr's describes the write buffer to temporary store write data request (zumkerhr's Fig 3: #330).

As in claim 39, the claim recites wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus. Zumkehr further describes the write buffer in MMB is provided to temporary store data from host and thus decoupling the host to handle another accessing data on the memory bus (Zumkehr's Fig 5)

As in claims 41-43, the claims recite wherein bypassing the read data on the memory bus comprises decoupling the write data from the memory bus for a time period to avoid data collision on the memory bus (claim 41); temporarily storing the write data in a bypass buffer during the receipt of the read data (claim 42); wherein providing the write data to the memory bus comprises providing the write data through at least one memory module of the memory system before decoupling the write data from the memory bus (claim 43). The claims rejected

based on the same rationale as in the rejection of claim 39. Zumkehr's Fig 5 clearly describes the write FIFO to store the write data temporary while allowing read data from sdram to host to be sent over the data link.

As in claim 40, the claim rejected based on the same rationale as in claim 5. Furthermore Zumkehr describes the translator hub can receive a read, and a write commands, for example from host, into its request queue and processing these commands and the returning read data from memory device to host in an interleaving and efficiently usage of the bus throughput (Zumkehr's column 5 lines 1-10 FIFO queue, allowing host to schedule multiple read write requests).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bogin et al US 6523093.

Kapur et al US 6912612.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DD

Mano Padmanabhan 8/5/06

Supervisory Patent Examiner

TC2188

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER